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Improved Methods of Forming Monolithic Integrated Circuits Having Complementary Bipolar Transistors

Two new processes form complementary (NPN and PNP) transistors in monolithic semiconductor circuits, require fewer steps (infusions) than previous methods, and eliminate such problems as nonuniform h_{FE} distribution, low yield, and large device formation. Such large devices often resulted from attempts to form integral passive components because the high level of doping required produced very low sheet resistance in the area where resistors were to be formed.

Both of the new processes employ the concept of a buried layer (N+). The novelty of this concept lies in using the buried layer as a diffusion stop, rather than following the more conventional idea of reducing saturation resistance. Both processes achieve well-matched complementary transistor pairs with improved yield rates. In addition, one of the processes buries the P-type impurity, which forms the PNP collector and the P-N junction isolation, as well as the N-type diffusion stop. The material is then diffused upward through the epitaxial layer, resulting in low concentration at the surface and high sheet resistance (approximately 550 ohms/cm²).

Note:

Requests for further information may be directed to: Technology Utilization Officer

Langley Research Center Hampton, Virginia 23365 Reference: TSP71-10035

Patent status:

Inquiries about obtaining rights for the commercial use of the invention may be made to:

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